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Three-dimensional radio-frequency transformers based on a self-rolled-up membrane platform

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Radio-frequency (RF) integrated circuits are used for wireless communications and require transformers capable of transferring electrical energy at RF/microwave frequencies. Traditional on-chip RF transformer designs have complex fabrication schemes and offer limited performance scalability. Here we report on-chip RF/microwave transformers that are based on a self-rolled-up membrane platform. The monolithic nature and versatility of this platform allows us to create high-performance transformers while maintaining an ultra-compact device footprint and by using only planar processing. We also show that the performance of the three-dimensional RF transformers improves with scaling, which is in contrast to conventional planar designs. In particular, we observe a continuous rate of increase in the index of performance of our RF transformers as we scale up the turns ratio. This behaviour is attributed to the almost ideal mutual magnetic coupling inherent to the self-rolled-up membrane three-dimensional architecture.

The Internet of Things (IoT) is a continually growing, massive communication network composed of wireless transceivers and sensors[1–3]. On-chip transformers are important elements in IoT devices, with applications in energy converters, fluxgate magnetometer sensors, wireless pressure sensors, and bioparticle detectors in microfluids, as well as traditional uses in wireless transmitters for signal amplification, impedance matching, d.c. signal isolation and low-noise feedback[4–7].

The ideal performance characteristics of on-chip transformers include a wide range of turns ratios (n), a high magnetic coupling coefficient (k_{im}), electrical and mechanical independence of the substrate, and small chip area (S), allowing high inductance density and low fabrication cost. In practice, the design and fabrication of on-chip transformers must be compatible with standard complementary metal–oxide–semiconductor (CMOS) or compound semiconductor technologies to realize a high level of integration and low production cost. Currently, there are three common on-chip transformer configurations: interleaved, tapped and stacked. Each of these configurations offers different trade-offs in terms of self-inductance, magnetic coupling coefficient, intercoil and coil-to-substrate capacitance, self-resonant frequency and chip area (see Supplementary Table 1 for a summary of the attributes of these three common on-chip transformer configurations)[8].

These trade-offs result from the layer-by-layer two-dimensional (2D) processing flows, which limit the shape of the coils to a single plane and make it difficult to obtain a large turns ratio without degrading the magnetic coupling coefficient. One solution to this problem is to embed multilayer coils in the substrate and stack them vertically, although this requires complicated processing. Issues such as low self-inductance density and substrate parasitic effects are also associated with the planar coil structure[9–11].

For IoT applications, conformal electronics on soft substrates have become prevalent. These require passive electronics to be mechanically flexible on a deformable substrate[12]. On-chip transformers designed in a planar configuration are unable to meet these new specifications because their electromagnetic (EM) field distribution is sensitive to structural parameters. Various technologies have been proposed to construct on-chip transformers based on 2.5D (multiple layers stacked in the vertical direction with negligible thickness compared to the device footprint in-plane) or 3D coils. For on-chip radio-frequency (RF)/microwave air-core transformers, technologies include implementing multiple layers for the primary and secondary coils or using automatic wire bonding fabrication in conjunction with traditional microelectromechanical systems (MEMS) processing[5,10,13–17] are reported. For power magnetic-core micro-transformers, existing technologies include automatic and high-speed wire-winding and wire-bonding fabrication processing[18–21]. All of these approaches improve the electrical performance by creating a relatively high coil density, but still suffer from either the drawbacks of the 2D design framework or complicated fabrication schemes.

In this Article we demonstrate on-chip RF transformers consisting of two sets of rolled-up coils, which are formed monolithically using a self-rolled-up membrane (S-RUM) nanotechnology platform. These devices exploit the efficient spatial configuration of 3D primary and secondary windings for superb magnetic mutual induction. With respect to the current state of the art for air-core RF/microwave on-chip transformers (summarized in Table 1), we show that the S-RUM platform technology can overcome fundamental challenges in planar transformers to achieve large turns ratios, large coupling coefficients and high maximum working frequencies, simultaneously with a miniaturized footprint and high fabrication yield.

S-RUM nanotechnology

S-RUM technology, specifically the SiN_x-based platform, has recently provided a new approach for the design of on-chip components in electronics, photonics and bioengineering[22–30]. Briefly, this technology enables the formation of 3D tubular structures via self-assembly of strained 2D nanomembranes as they are released from the substrate by etching the sacrificial layer. In general, the membrane structure of S-RUM transformers can include multiple

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Table 1 | Comparison of RF/microwave on-chip air-core transformers.

Work	Coil configuration	Turns ratio	Maximum inductance	Maximum Q factor	Magnetic coupling coefficient	Footprint	Maximum working frequency	Index of performance[a]	Special processing
Ref. 9	Bifilar integrated spiral	1.94	2.8 nH	8@10 GHz	0.6	0.09 mm^2	>10 GHz	12.9 mm^{-2}	Substrate transfer
Ref. 10	Interleaved integrated spiral	1.026	4 nH	8@4.6 GHz	0.66	0.11 mm^2	10.1 GHz	6.16 mm^{-2}	Microporous silicon substrate
		1.304	3.4 nH	8.4@4.7 GHz	0.62	0.0784 mm^2	12.9 GHz	10.31 mm^{-2}	
		1.944	3.4 nH	8.4@5.3 GHz	0.44	0.0784 mm^2	13.4 GHz	10.9 mm^{-2}	
Ref. 45	Interleaved integrated spiral	1.228	2.98 nH	7.1@4.6 GHz	0.65	0.0441 mm^2	9.68 GHz	18.1 mm^{-2}	Patterned ground shield
		1.641	2.98 nH	NA	0.59	0.0441 mm^2	9.4 GHz	22 mm^{-2}	
		2.696	2.98 nH	NA	0.41	0.0441 mm^2	8.57 GHz	25.1 mm^{-2}	
Ref. 13	Multilayer integrated spiral	1	12.9 nH	NA	0.99	0.01 mm^2	6 GHz	99 mm^{-2}	Multiple metal layers embedded in substrate
		2.11	12.9 nH	NA	0.93	0.01 mm^2	5.3 GHz	195.77 mm^{-2}	
		2.95	12.9 nH	NA	0.83	0.01 mm^2	5.2 GHz	245 mm^{-2}	
		4.2	12.9 nH	NA	0.69	0.01 mm^2	5.15 GHz	288.75 mm^{-2}	
		4.69	12.9 nH	NA	0.61	0.01 mm^2	4.8 GHz	288.03 mm^{-2}	
		5.68	12.9 nH	NA	0.48	0.01 mm^2	5.5 GHz	270.97 mm^{-2}	
This work	Self-rolled-up membrane integrated 3D spiral	1.48[b]	0.55 nH	1@7 GHz	0.7	0.003 mm^2	20 GHz	344 mm^{-2}	None
		1.78[b]	0.51 nH	0.8@7 GHz	0.86	0.003 mm^2	13.5 GHz	509 mm^{-2}	
		2.5[b]	0.55 nH	1.1@7 GHz	0.95	0.003 mm^2	>20 GHz	789 mm^{-2}	
		1.87[c]	1.1 nH	1.6@7 GHz	0.79	0.008 mm^2	11.5 GHz	185 mm^{-2}	

[a]Index of performance = (turns ratio × magnetic coupling coefficient)/footprint. [b]Type A design S-RUM transformer samples in this Article. [c]Type B design S-RUM transformer sample in this Article. Arrows indicate increasing direction of data value. NA: data not available.

layers of dielectric and conductive thin films[31,32]. Each layer can be under different stress, and the polarity (compressive or tensile) and magnitude of the stresses depend on the deposition methods, such as evaporation (thermal or electron beam), atomic layer deposition (ALD) and plasma-enhanced chemical vapour deposition (PECVD), and conditions employed. The thin film stack can be classified into one of two categories: the strained rolling vehicle, which provides the main rolling force, and the functional thin films, which provide electrical/optical/biomedical performance. The coiling effect is determined by the stress imbalance from the whole stack of thin films (see Supplementary Information Section 3 for more analysis). The dimensions of the rolled-up membranes can be precisely calculated by quasi-static finite element method (FEM) simulation[33,34]. By pre-patterning and depositing conductive layers on top of a strained bilayer SiN_x nanomembrane, complex hierarchical 3D architectures can be obtained[31,35]. The conductive layer (metal, for example) contributes to the major rolling resistance in most cases, which is determined by its Young's modulus and thickness. The larger the Young's modulus and thickness, the more rolling resistance the conductive layer has. For better conductivity, the thickness of the metal is expected to be sufficiently large to not significantly degrade the conductivity compared to that of the bulk counterpart.

The S-RUM platform allows the fabrication of on-chip inductors from 2D planar to 3D tubular structures without violating planar processing flows. In addition to the simplicity of achieving a high density of coils, the 3D up-standing microtube platform naturally offers the advantage of minimal electromagnetic field interaction with the underlying substrate. S-RUM inductors have been reported previously with enhanced inductance density and excellent immunity to parasitic substrate effects[27,33,36]. However, several major issues must be resolved before the S-RUM platform becomes a mainstream technology for on-chip passive components, including the lack of a general design rationale, the limitation of the conductive material being exclusively noble metals, the low fabrication yield of more complex hierarchical architectures, and the unknown mechanical and thermal stability of S-RUM structures for further packaging and applications in extreme environments. Preliminary results on S-RUM-based transformers have been reported in conference proceedings[37–39]. Here, we report practical 3D on-chip RF transformers and comprehensively study their mechanical–electrical relationships to establish general design rationales.

Fabrication and design

Figure 1 shows the step-by-step three-level S-RUM process flow used for the fabrication of on-chip air-core transformers on a Si substrate (see Methods for details). Briefly, a Ge sacrificial layer was deposited by electron-beam evaporation, which is known to produce fairly smooth Ge films on a SiO_2 isolated silicon substrate, followed by depositing an oppositely strained silicon nitride (SiN_x) bilayer (Fig. 1a). The sacrificial layer thickness uniformity and smoothness directly affect the membrane releasing rate across the etch front, impacting the yield of coherent rolling. The layered stack was then etched down to SiO_2 by reactive ion etching (RIE) to form a mesa (Fig. 1b). Next, a metal layer (consisting of 5 nm Ni and 30–150 nm Au (or Cu, Al, Co)) was deposited, followed by photolithography patterning to form the primary and secondary coils simultaneously (Fig. 1c). A 10- to 30-nm-thick Al_2O_3 thin film layer was then deposited by ALD to serve as the cover layer (Fig. 1d),

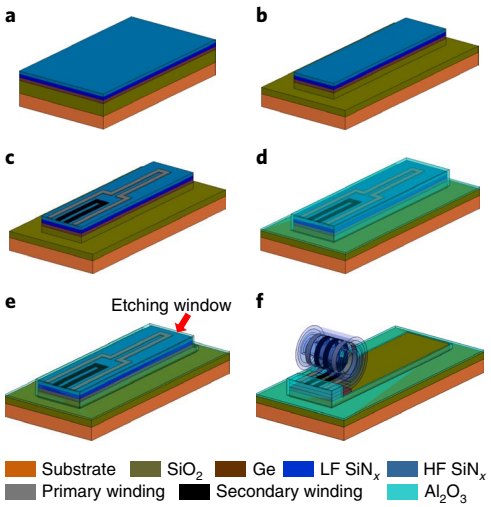

Fig. 1 | Schematic illustration of the 3D S-RUM transformer fabrication process flow. a, Deposition of SiO_2, Ge, low-frequency (LF) SiN_x and high-frequency (HF) SiN_x layers in sequence on a substrate. **b**, First lithography step to define a mesa by RIE. **c**, Metal layer deposition by electron-beam evaporation and second lithography step to define the metal pattern. **d**, Al_2O_3 cover layer deposition by ALD. **e**, Third lithography step to define an etching window. **f**, Removal of Ge sacrificial layer by H_2O_2 wet etching to trigger the self-rolling process of the stacked membrane. All materials are colour-coded as indicated in the key.

and an etch window was opened (Fig. 1e). Upon removing the Ge sacrificial layer through the etch window laterally, grey-coloured (in Fig. 1d) planar strips rolled up to form the primary coil while black-coloured (in Fig. 1d) planar strips became the secondary coil. The final configuration of the primary and secondary coils contained a fully overlapped centre part and two non-overlapped side parts (Fig. 1f). Unlike previously reported S-RUM process flows[26,27], the SiN_x cover layer was replaced by an ALD Al_2O_3 cover layer (Fig. 1d). This change in the process flow liberates the choice of conduction layer materials from only noble metals to all metals in use in the integrated circuit industry including Cu, and also solves the inherent pinhole issue with the SiN_x bilayer.

Unlike conventional on-chip planar passive electronics, the design of S-RUM on-chip transformers must consider both the horizontal layout (Fig. 2a) and vertical layer stacking (Fig. 1a). Specifically, the vertical membrane structure, including material properties and the thickness of each layer, determines the inner diameter after the device is rolled up, and the horizontal layout determines the spatial configuration, such as the number of turns of the primary and secondary coils and the spacing between them. The horizontal layout shown in Fig. 2a, where dimensional parameters are labelled, shows the simplest layout design with the minimum number of cells for each coil (w_{sp}, w_{ss}, w_{cp} and w_{cs} represent the width of the primary and secondary coil strip and the width of the connection lines of the primary and secondary coils, respectively; l_{sp}, l_{ss}, l_{cp} and l_{cs} represent the length of the primary centre cell and secondary coil strip and the length of the connection lines of the primary and secondary coils, respectively; g_v and g_l represent the gap between the secondary coil and the primary centre cell and the gap between the secondary coil and the primary side cell, respectively). For testing purpose, one of the two ports of both the primary and secondary coils are connected to the electrical ground to enable a two-port measurement. Note that each rolled-up metal strip is called a 'coil cell', or a 'cell', and cells are connected in series to form a coil, as indicated in Fig. 2b.

As the planar device membrane rolls up to enable new spatial configurations in the third dimension, it also introduces an additional degree of complexity in the electrical relationship between the primary and secondary coils. Figure 2b shows a schematic view of the rolled-up device coil structure with critical parasitic parameters, represented by C_{cp}, C_{cs}, C_{cps}, C_{oxp}, C_{oxs}, C_s and R_s (as labelled). The inductance of the primary coil is the sum of the self-inductance of the side cells and centre cells and the mutual inductance between them. All the side cells and centre primary cells are magnetically coupled to the secondary coil, but have different intercell cross-coupling capacitances (C_{cs} and C_{cp}). The intercoil cross-coupling capacitance (C_{cps}) is determined by the overlap area and the gap between the centre primary and secondary coils. The rolled-up primary and secondary coils interacting with the doped substrate form parasitic capacitance across the oxide layer (C_{oxp} and C_{oxs}). The electromagnetic field penetrating the substrate introduces substrate parasitic capacitance (C_s) and eddy current loss modelled by resistance R_s. All these parasitic capacitance parameters are unique and critical in such a 3D primary and secondary coil overlapping configuration and cannot be ignored.

Our design approach starts with establishing the underlying relationship between the electrical performance and the geometrical dimensions in the horizontal layout and vertical membrane structure, according to a general design rationale illustrated in Fig. 2c. Theoretical modelling by quasi-static FEM[33] serves as the basis for the horizontal layout design. The focus is on calculation of the inner diameter and then the number of turns of the primary and secondary coils according to the turns ratio and inductance requirements, using analytical EM modelling for a standalone rolled-up coil[26]. If the design fails to meet desired specifications by FEM 3D EM simulation, we consider changing the inner diameter by redesigning the vertical membrane structure or optimizing the horizontal layout. Otherwise, the design proceeds to fabrication and on-chip testing. This loop is repeated until all devices meet the specified requirements. During the iterations, studying the deviation between the design and experimental results and using the feedback for further dynamic horizontal layout optimization are critical.

Using this systematic, computationally guided design approach, a diverse set of the S-RUM on-chip transformer structures were designed, fabricated and tested. Figure 2d–g presents an example of the high-precision mechanical and electrical simulation and the corresponding device fabrication and testing results. Figure 2d shows a simulated rolled-up membrane structure consisting of the layered material stack, resulting in an inner diameter of 50 μm (the dynamic rolling process is shown in Supplementary Video 1). The measured inner diameter of the corresponding fabricated device shown in Fig. 2e matches the simulated value perfectly. Figure 2f shows the 3D EM model of the device and the spatial distribution of the magnetic field vectors at 1 GHz with phase equal to zero degree (the dynamic H field distribution is shown in Supplementary Video 2). Very low EM field leakage to the substrate is observed, implying that the substrate's parasitic effect is minimal. Also, the S parameters obtained from the EM FEM simulation match very well with the measured data, as shown in Fig. 2g. A comprehensive comparison of the extracted simulated performances and the tested results is presented in Supplementary Table 3. These results validate the mechanical–electrical FEM analysis, which accurately predicts the performance of S-RUM on-chip transformers from the beginning of the membrane structure design phase, and establishes the relationship between performance and material properties. More details of the EM FEM simulation are provided in the Supplementary Information Section 5.

Fabrication controllability and robustness characterization

We fabricated S-RUM transformer device samples with two different layered material stack structures, each including variations

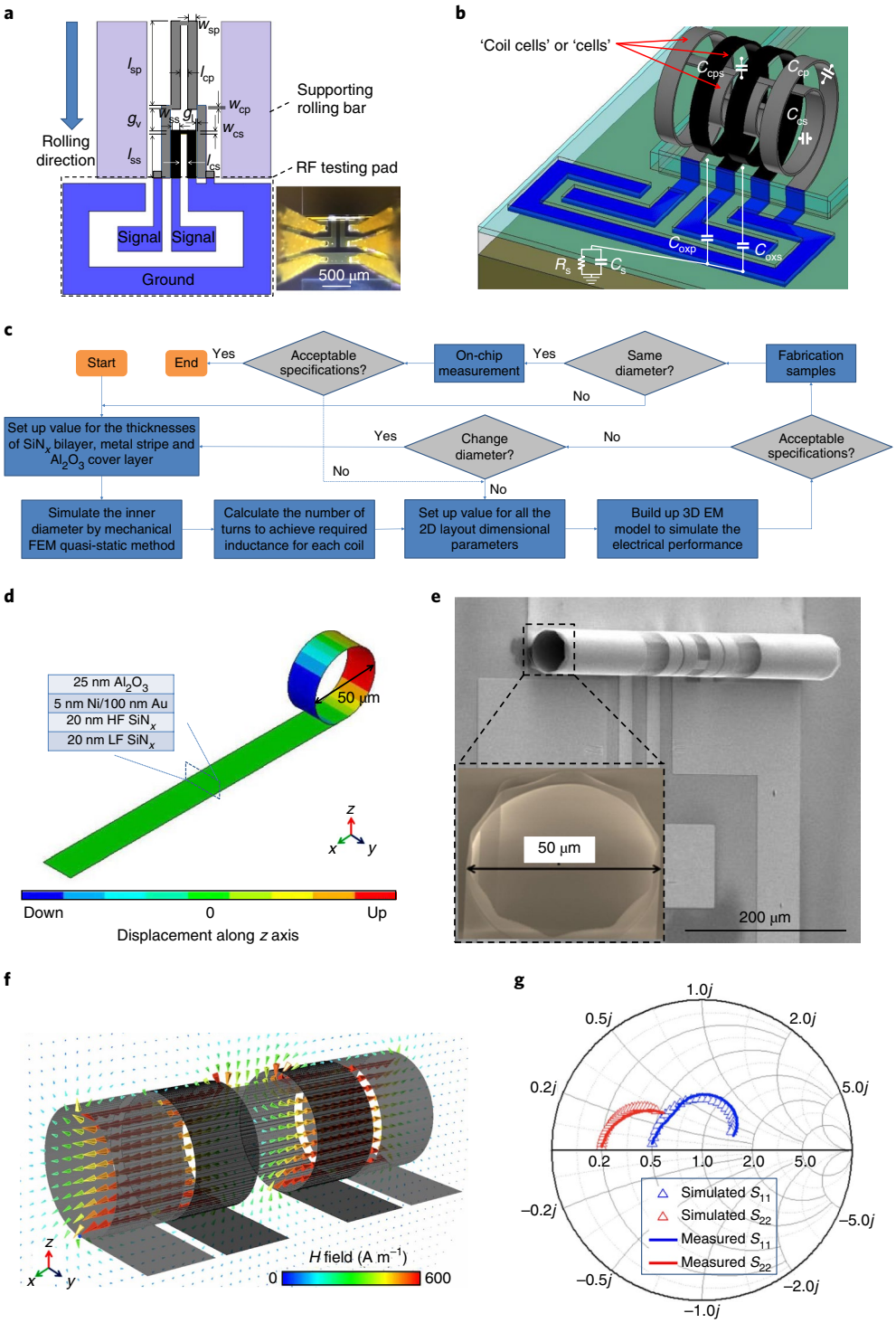

Fig. 2 | S-RUM transformer design layout and fabrication results. a, S-RUM transformer layout design with dimensional parameters and RF testing pads labelled. Primary and secondary coils are colour-coded grey and black, respectively. RF testing pads are designed for a ground–signal–ground (GSG) probe configuration. Inset (lower right): fully fabricated device under RF test with six probes contacted on the ground and signal pads. **b**, Schematic of the rolled-up 3D transformer structure from the planar layout in **a** with parasitic parameters and 'coil cells' labelled. Parasitic effects of testing pads will be calibrated out. **c**, Illustration of the entire design flow chart for S-RUM micro-transformers. **d**, A modelled S-RUM tubular structure rolled-up from the stacked layer structure indicated, with an inner diameter of 50 μm, using a quasi-static FEM mechanical simulation method. **e**, Tilted scanning electron microscopy (SEM) image of the fabricated S-RUM transformer sample based on the design in **d**. The wide strips on both sides of the tube are supporting rolling bars, as indicated in **a**. Inset: cross-sectional view with the inner diameter labelled. **f**, Electromagnetic FEM simulated *H* field distribution at 1 GHz on the cross-sectional *x*–*z* plane, which symmetrically cuts through the tubular structure. **g**, Simulated versus measured *S* parameters of the transformer sample in **e**.

of several types of horizontal design, to obtain S-RUM on-chip transformers with a wide range of dimensions and perfor1mance specifications. Design A has 5 nm Ni/60 nm Au/10 nm Al_2O_3 in the layered stack, and Design B has 5 nm Ni/100 nm Au/25 nm Al_2O_3 in the structure. Design A has two different types of horizontal layout: Type A1, four-cell primary coil, two-cell secondary coil; Type A2,

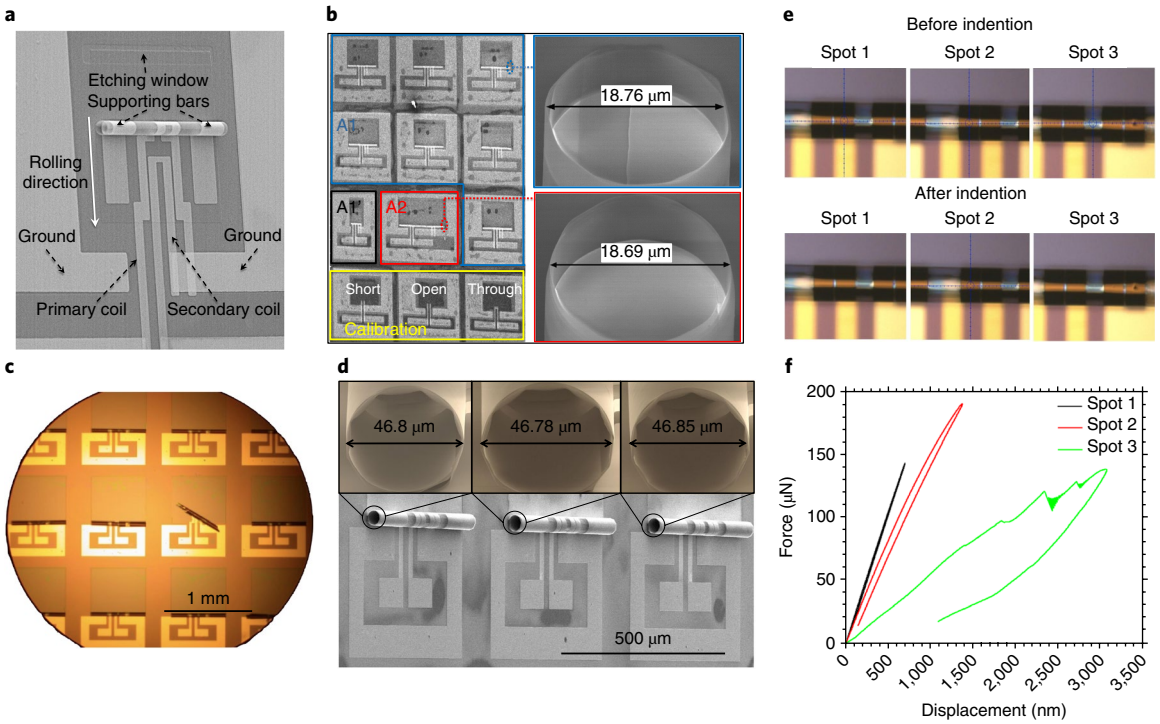

Fig. 3 | Fabrication controllability, and thermal and mechanical stabilities of the S-RUM micro-transformers. **a**, Tilted SEM image of a Type A1 sample partially rolled up, showing the transition of the 2D primary and secondary strips to 3D coils. **b**, Tilted SEM images of an S-RUM transformer array, with a similar structure to the one shown in **a** and 100% fabrication yield, consisting of various Design A samples and on-chip measurement calibration structures. Blue box: Type A1 samples; red box: Type A2 sample; black box: Type A1 sample without supporting bar, A1'; yellow box: calibration structures (from left to right: short, open and through). Upper right images: zoomed-in cross-sectional views of Samples A1 and A2, with identical inner diameters of ~18.7 μm. **c**, Optical image showing a high-yield S-RUM transformer array (Design B). **d**, SEM images of S-RUM transformer samples after annealing at 350 °C in an N_2 environment for 5 min. Insets: cross-sectional views with identical inner diameters. **e**, Top-view optical images before and after nano-indention with different spots along the axis of the S-RUM transformer sample indicated. Spots 1, 2 and 3 are on top of one of the centre metal coils, the other centre metal coil, and the SiN_x membrane, respectively. Nano-indention was carried out after the sample was annealed at 350 °C. **f**, Plot of displacement versus force for Spots 1 to 3.

ten-cell primary coil, eight-cell secondary coil. Design B has a single horizontal layout: Type B1, four-cell primary coil, two-cell secondary coil. Both Type A1 and B1 have several combinations of lengths l_{sp}, l_{ss} and g_v (for details of sample dimensions see Supplementary Information Section 6).

Figure 3 shows a series of as-fabricated S-RUM transformer devices with different designs and thermal and mechanical stability test results. Figure 3a presents a Type A1 S-RUM on-chip transformer captured during rolling with various parts of the structure labelled, showing how the 2D primary and secondary strips transition to 3D coils. As the rolling continues, the primary and secondary coils will become more and more overlapped in their 3D spatial configuration to ensure magnetic field coupling. The fabrication yield of Type A1 samples (outlined by the blue box in Fig. 3b) and A2 sample (red box) reaches 100% yield. The sample shown in the black outlined box (A1') is designed without the supporting side bars, which were originally designed to avoid misalignment of the rolled-up coils, but its successful rolling suggests the possibility of abandoning the supporting bars in further optimized iterations. Recall that the diameter is determined by the vertical layer stack thickness and stress, so all Type A samples should have the same diameter, and Type B should have a small diameter due to the reduced thickness of the membrane structure, as designed. The right-side SEM images in Fig. 3b show the measured inner diameters for both Type A1 and A2 samples, which are almost identical (~18.7 μm), but much smaller than that of Type B1 (shown in Fig. 2e), demonstrating the excellent process controllability. Close examination of the cross-sectional views of Figs. 2e and 3b also reveal that the coils are tightly rolled up without any air gap between the turns, which is extremely important for high performance tolerance. Figure 3c presents a top-view optical microscope image of an S-RUM on-chip transformer array based on Design B with 11 of 12 devices successfully fabricated. The device second from the right in the centre row is distorted before finishing rolling due to a pinhole issue in the PECVD SiN_x bilayer. Compared to previously reported S-RUM inductors, with fabrication yields less than 50%[27], all these fabrication results demonstrate the effectiveness of the new fabrication process flow that includes the additional ALD Al_2O_3 cover layer in significantly overcoming the pinhole issue.

To test the thermal stability of the S-RUM transformers, annealing tests were carried out at temperatures close to the SiN_x film deposition temperature (250 °C) and beyond (350 °C) for 5 min on samples based on Design B. The inner diameter showed no change at 250 °C, but shrank to ~46.8 μm (Fig. 3d) from 50 μm (Fig. 2e) at 350 °C, presumably as a result of out-diffusion of the embedded hydrogen and ammonia within the SiN_x film[31]. Note that even with the ~6.4% change in inner diameter, the coils are still very tightly rolled up together, with no observable fracture or film damage. Cross-sectional images of devices are compared in Fig. 3d, where three samples after annealing at 350 °C are shown to have nearly identical reduced inner diameters as labelled. This indicates that even after being annealed at high temperature, the transformer samples still have highly uniform structures.

The S-RUM transformer samples, after the rapid thermal annealing (RTA) at 350 °C, were then subjected to a mechanical stability test with different maximum indentations and forces at

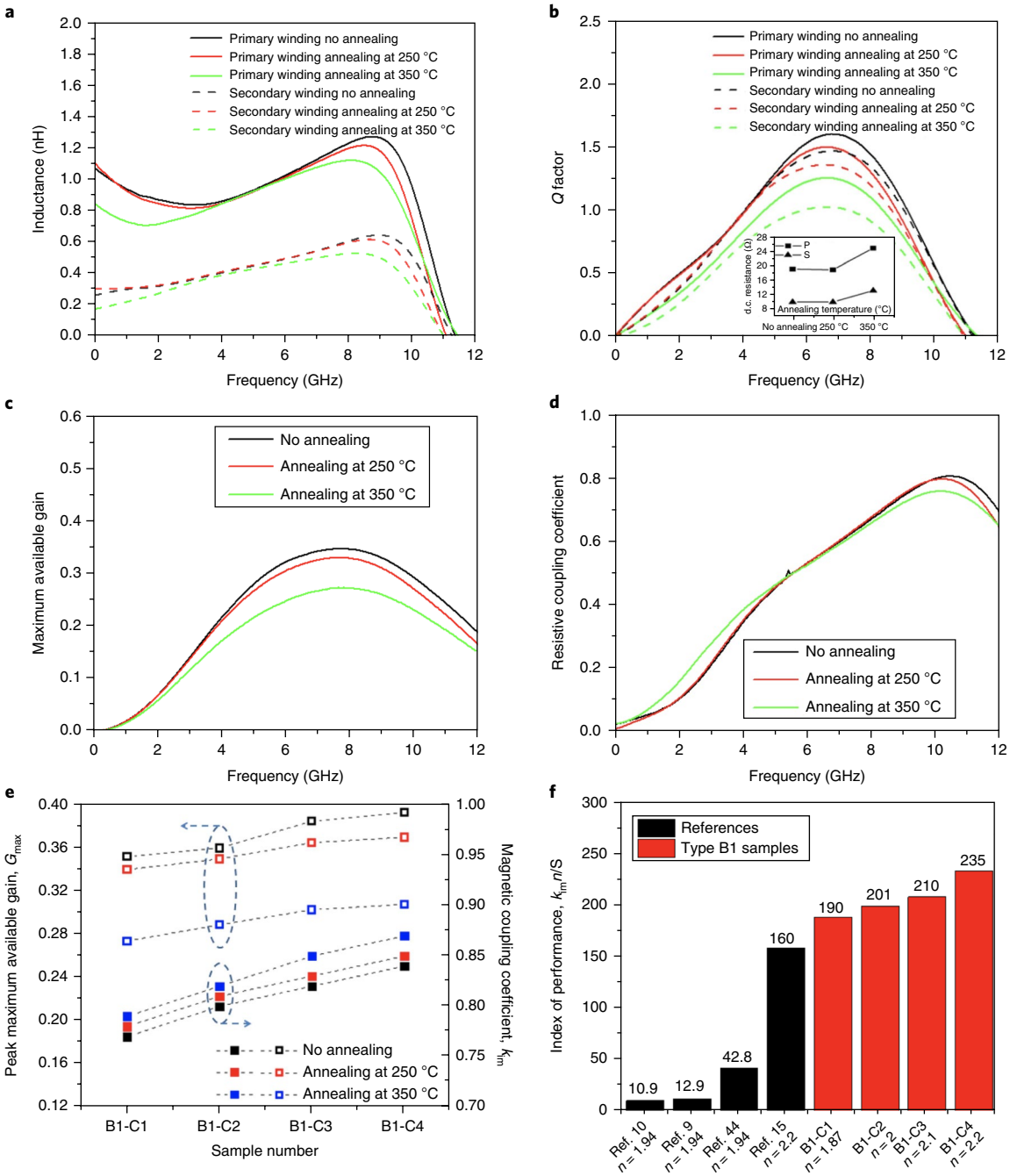

Fig. 4 | Performance of S-RUM transformers before and after thermal annealing for Sample B1-C1, and the index of performance benchmarking with literature counterparts. a, Inductance versus frequency of the primary and secondary coils. **b**, *Q* factor versus frequency of the primary (P) and secondary (S) coils. **c**, Maximum available gain G_{max} versus frequency. **d**, Resistive coupling coefficient versus frequency. **e**, Comparison of peak maximum available gain G_{max} and magnetic coupling coefficient k_{im} among Type B1 samples. **f**, Benchmarking the index of performance $k_{im}n/S$ among Type B1 samples and on-chip planar counterparts in refs [9,10,15,44].

several spots along the microtube axis (Fig. 3e). The load versus displacement characteristics were compared for three spots positioned at the top of a centre metal coil (Spot 1), a side metal coil (Spot 2) and between the coils (that is, the SiN_x membrane alone, Spot 3), as indicated in Fig. 3e. It can be seen from Fig. 3f that the structures at all the spots under testing experienced continuous fracturing with increasing indention force. Before the first fracturing point, all structures stayed in the elastic deformation regime. Stiffness values for different spots in the elastic region were calculated to be 210.2, 164.8 and 53.2 N m^{-1}, respectively, with the maximum stiffness at the centre coil location, and only weakened slightly at the side coil location, while the stiffness reduced by ~4× for locations between the coils. Notably, the maximum stiffness of the sample tested here is 375.4 times larger than for a suspended MEMS high-*Q* factor spiral inductor with X-beams, which had a maximum stiffness of ~0.56 N m^{-1} at its inner turn and was claimed to have enhanced the maximum mechanical strength by more than 4,500× compared with other MEMS suspended inductors[40]. The stiffness of the S-RUM on-chip transformers could be even greater when the coils are designed to have more turns for higher inductance. The large stiffness of the S-RUM transformer structure implies the device has some degree

of mechanical flexibility when directly subjected to external force during packaging or undergoing a shock with large g force (see discussion in Supplementary Information Section 9).

The robustness of these S-RUM on-chip air-core transformers towards both thermal and mechanical stability ensures a high feasibility of device packaging and suggests possible applications in extreme environments with high temperature and large g forces.

Characterization and performance of S-RUM transformers

We focus here on the characterization (see Methods for details) and analysis of the electrical performance of Sample B1-C1, as it had the best overall electrical performance out of all the designs fabricated and tested. Descriptions of the electrical performance of other samples are provided in the Supplementary Information Section 8.

Figure 4a,b presents the measured temperature-dependent inductance and Q factors of the primary and secondary coils, respectively, before and after annealing at 250 °C and 350 °C. The inductances of the primary coil and the secondary coil are ~1.08 nH and ~0.27 nH at low frequency, respectively, and then vary depending on the frequency due to parasitic capacitances, including C_{cp}, C_{cs} and C_{cps}. The resonant frequencies of all coils are beyond 11 GHz. At 7 GHz, the maximum Q factors are ~1.65 and ~1.45 for the primary and secondary coils, respectively. After annealing, for inductances, it is clear that there is hardly any change at 250 °C, but a noticeable decrease at 350 °C, especially at frequencies lower than 4 GHz. The Q factors degrade accordingly and a more substantial drop of Q_{max} after 350 °C annealing can be seen, which can be attributed to the increase in Au resistivity. As shown in the inset of Fig. 4b, the d.c. resistances of both primary and secondary coils are stable until annealed at 350 °C, where the Au film experiences compressive stress as the tube deforms and the diameter shrinks.

Figure 4c shows the maximum available gain G_{max}, which is indicative of the overall performance by elucidating the energy loss in the primary and secondary coils as a function of frequency. For on-chip transformers, equation $G_{max} = 1-2(\sqrt{x^2+x}-x)$ was used to calculate the maximum available gain, where $x = (1-k_{re}^2)/(k_{im}^2 Q_p Q_s + k_{re}^2)$, and Q_p, Q_s and k_{re} are the Q factors of the primary and secondary coil and the resistive coupling coefficient, respectively[41]. The peak value of G_{max} occurs at the frequency where Q factors of both primary and secondary coils reach their maximum values. As shown in Fig. 4c, the maximum G_{max} for this sample reaches ~35% at 7.9 GHz without annealing, which corresponds to a magnetic coupling coefficient k_{im} of ~0.828. Annealing at 350 °C significantly decreased the maximum available gain (G_{max}) to 27.3% at 7.9 GHz but with a slightly increased magnetic coupling coefficient k_{im} of ~0.835, probably resulting from the shrinking inner diameter. Figure 4d shows the extracted mutual resistive coupling coefficient k_{re} as a function of frequency at different annealing conditions. k_{re} was calculated as $k_{re} = \mathrm{Re}(Z_{12})[\mathrm{Re}(Z_{11})\mathrm{Re}(Z_{22})]^{-1/2}$, which mainly accounts for the hybrid effects of parasitic capacitances and eddy currents in the silicon substrate[9,42]. The lower the k_{re}, the less substrate parasitic effects the transformer has. Notably, even though all S-RUM transformers were fabricated with only a 0.8-μm-thick SiO_2 insulation layer (in standard CMOS, the SiO_2 layer separating passives from the substrate is >5 μm) on a standard doping range silicon substrate, the peak k_{re} value of ~0.8 is still smaller than that of most reported on-chip planar transformers, which is usually larger than 0.9 (refs [9,13,42]). This is because the majority of the EM field in the S-RUM structure is confined away from the substrate by design. The shrunken inner diameter after annealing at 350 °C further reduces the projection area on the substrate, and the substrate effects to a peak k_{re} value of ~0.76.

Figure 4e summarizes the maximum available gain G_{max} and the corresponding magnetic coupling coefficient k_{im} for all Type B1 samples before and after annealing. Type B1-C2, B1-C3 and B1-C4 samples are designed to have gradually increased length ratios of l_{sp}/l_{ss}, without altering the total length of the primary strip, meaning

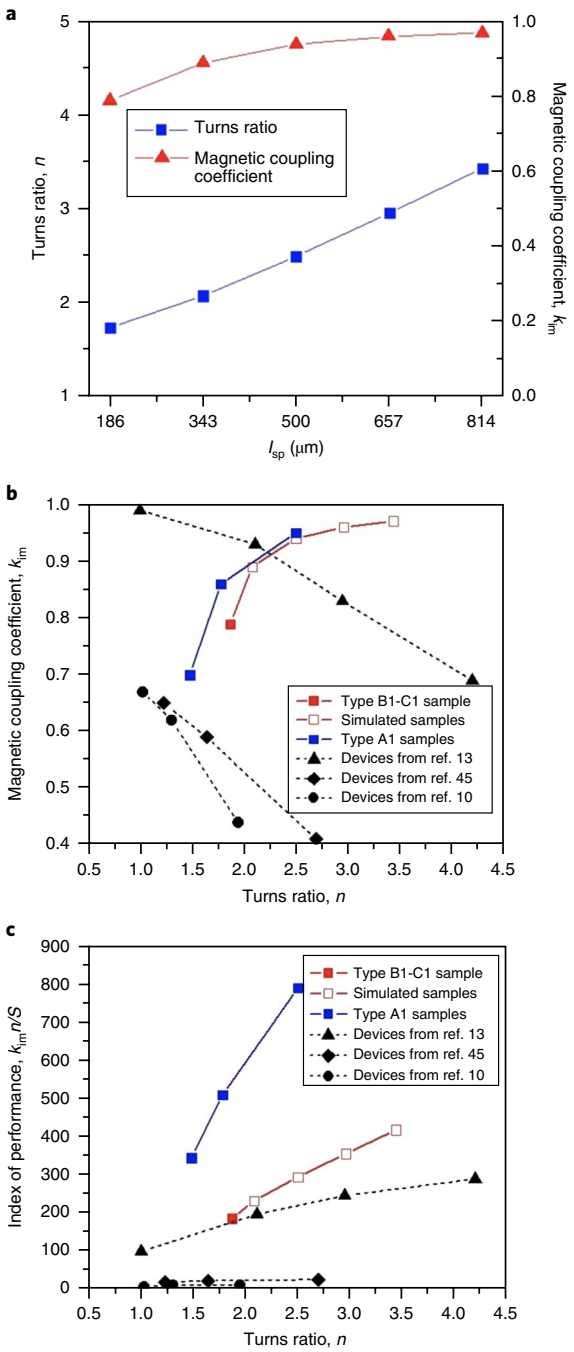

Fig. 5 | Extended performance comparison between on-chip S-RUM air-core RF/microwave transformer tested and simulated samples and their planar on-chip counterparts in the literature. a, Simulated performance improvement of the S-RUM air-core transformers based on Sample B1-C1 by only increasing the length of the centre cell strip of the primary coil with a step of one turn. **b**, Magnetic coupling coefficient k_{im} versus turns ratio n. **c**, Index of performance $k_{im}n/S$ versus turns ratio n.

that the centre cell has more turns than the side cells although the total number of turns is fixed. Therefore, more mutual magnetic coupling occurs in the centre overlapping area, giving a magnetic coupling coefficient k_{im} gradually increasing from 0.78 to 0.87, and the corresponding peak maximum available gain G_{max} increasing from 0.35 to 0.39. When the diameter becomes smaller after annealing, the number of turns for both primary and secondary coils effectively increases. With the unchanged separation distance

between coils, more turns per coil means stronger mutual magnetic coupling. Therefore, for all Type B1 designs, k_{im} slightly increases as a result of the fractional increase of number of turns with annealing, but G_{max} still drops, especially after annealing at 350 °C, because the inductance and Q factor deteriorate significantly.

Figure 4f benchmarks the indices of performance[13,43] for S-RUM transformer Type B1 samples and planar counterparts from the literature[9,10,15,44] by comparing the value of $(k_{im}n)/S$ relative to turns ratio n. Sample B1-C4 shows a value of $(k_{im}n)/S$ of ~235, which represents an enhancement of 47% over that of a state-of-the-art planar transformer with the same turns ratio of 2.2 (ref. [15]). If the value from ref. [15] is excluded from comparison as it requires much more complex fabrication processes and expensive lithography mask set, our S-RUM on-chip transformer B1-C1 is ~4.44 times better than the best planar counterpart (comparing S-RUM Sample B1-C1 with the device reported in ref. [44]).

We further explored the scalability of S-RUM on-chip transformers for larger turns ratios, larger indices of performance, reduced intercoil capacitances for higher working frequencies, and larger self-inductances with a nearly unchanged footprint by simply extending the planar layout design space of the S-RUM architecture. Figure 5a presents four more simulated samples designed by continually increasing the length of the centre cell of the primary coil l_{sp} based on Sample B1-C1 with a value of l_{sp} of 186 μm. As can be seen, the mutual magnetic coupling in the centre area becomes dominant when more turns are added to the centre cells, implying that the magnetic coupling coefficient gradually becomes close to 1 and the turns ratio linearly increases with length of l_{sp}. The observation that the magnetic coupling coefficient gradually approaches the ideal value as the turns ratio increases is a result of the 3D construction of the primary and secondary coils.

The same trend is also found in Type A1 samples, as plotted in Fig. 5b. In contrast, the state-of-the-art on-chip transformers based on planar coil structures, which are plotted in Fig. 5b as black lines and symbols, clearly show opposite trends because of the inevitability of sacrificing the magnetic coupling efficiency when a large turns ratio is required[10,13,45]. Consequently, as shown in Fig. 5c the index of performance $k_{im}{\cdot}n/S$ continues to increase with turns ratio for S-RUM devices, but for the planar counterparts $k_{im}{\cdot}n/S$ gradually flattens or even decreases (as shown in Table 1 and ref. [13]; when the turns ratio increases from 4.69 to 5.68, the index of performance drops from 288.03 mm^{-2} to 270.97 mm^{-2}) as the turns ratio increases. This proves unambiguously that much better performance scalability with turns ratio can be achieved with the S-RUM platform for transformers. Furthermore, the improvement is more dramatic with a reduction of the inner diameter, as Type A1 samples show much larger indices of performance (with a maximum value of ~790) compared to that of Type B1 samples. Further reduction of the diameter can be realized by maximizing strain mismatch in the bilayer SiN_x membrane and the use of a high-conductivity strip material with thinner thickness, such as multilayer graphene.

Conclusions

We have reported RF/microwave air-core transformers based on a monolithic self-rolled-up membrane platform, and have systematically analysed their structural design, fabrication processing and electrical performance. The measured electrical performance of all samples showed turns ratios (n) from 1.5:1 to 2.5:1 and self-resonant frequencies from 11.5 GHz to over 20 GHz, and with device footprints (S) of 0.003 or 0.008 mm^2. The index of performance $((n{\cdot}k_{im})/S)$ of these samples reaches 235 at a turns ratio of 2.2:1, which represents an enhancement of 47% over the best on-chip planar counterpart reported so far for the same turns ratio. In contrast to planar counterparts, as the turns ratio (n) scales up, the coupling coefficient k_{im}, and thus the index of performance $((n{\cdot}k_{im})/S)$, continues to increase, indicating excellent performance scalability. This is because traditional on-chip air-core transformers manipulate the distribution and exchange of magnetic field only in 2D space, whereas the S-RUM design offers a third dimension in design. This ensures a much larger magnetic flux density surrounding the device and more efficient magnetic field exchange between the primary and secondary coils, leading to high mutual magnetic coupling with large inductance density. This inherent advantage of the self-rolled-up membrane 3D architecture can enable applications demanding extreme performance scalability, high frequency and deformation immunity.

We have also shown that the rolled-up SiN_x films are very stable both thermally and mechanically, which makes them promising for surviving packaging into integrated chips or as a standalone passive component, as well as potential feasibility for applications in extreme environments. A potential mechanical flexibility exists in these devices because the self-rolled-up membrane transformer stands above the substrate. The substrate could be readily bent perpendicular to the microtube axis of the self-rolled-up membrane transformer. The fabrication of self-rolled-up membrane transformers is fully compatible with all planar semiconductor processing, including CMOS (replacing Au with Cu or Al) and MEMS technologies, and it is also low in cost due to the simple fabrication requirement of three-step optical lithography, no special substrate treatment and small on-chip footprint. The electrical performance of the self-rolled-up membrane transformers could be further improved by simply adding more turns and cells to the primary coil and the secondary coils, and replacing the Au with higher-conductivity metals such as Cu, Co or even graphene. Such high-frequency self-rolled-up membrane on-chip transformers thus show significant promise for use in future IoT and wearable electronics applications.

Methods

Details of S-RUM transformer fabrication process flow. A 0.6-μm-thick SiO_2 layer was first formed by thermal oxidation for electrical isolation on a p-type Si substrate with resistivity of ~1–10 Ω cm. A 20-nm-thick Ge film was chosen as the sacrificial layer because of its smooth surface and relatively large Young's modulus, thus avoiding surface roughness accumulation and strain sharing, and was deposited by electron-beam evaporation. For its planar processing compatibility, low-temperature PECVD was used to grow the strained 'rolling vehicle', which included a 20-nm-thick low-frequency (LF, ~−1,168 MPa compressively strained, 360 kHz) silicon nitride (SiN_x) layer and a 20-nm-thick high-frequency (HF, ~406.95 MPa tensile-strained, 13.56 MHz) SiN_x layer deposited in sequence. The entire material stack is shown schematically in Fig. 1a. Freon RIE was then used to etch the layer stack into SiO_2 to form a mesa (Fig. 1b). The metal layer was deposited by electron-beam evaporation followed by photolithography patterning to form the primary and secondary coils simultaneously (Fig. 1c). This metal layer was a bilayer structure consisting of 5 nm Ni under the major highly conductive metal (Au, Cu and Al) with thickness from 30 nm to 150 nm, where Ni thin film was used as the adhesion and nucleation layer as well as the oxidation prevention layer to achieve a high-conductivity metal thin film. Next, a 10- to 30-nm-thick Al_2O_3 thin film layer was deposited by ALD (Fig. 1d); this served as a cover layer to avoid any oxidation of the conductive metal and protect the sacrificial layer from unwanted wet etching due to inherent pinhole issues within the SiN_x bilayer. A window was then opened down to the SiO_2 layer at the long end of the mesa opposite the contacts (Fig. 1e). On etching the Ge sacrificial layer, the grey-coloured (in Fig. 1d) planar strips rolled up to form the primary coil, while the black-coloured (in Fig. 1d) planar strips became the secondary coil. The final configuration of the primary and secondary coils contained a fully overlapped centre part and two non-overlapping side parts (Fig. 1f).

S-RUM transformer RF performance characterization. RF performance was measured using a Keysight E8363B PNA from 10 MHz to 40 GHz, and two port scattering parameters (S parameters) were obtained. An 'open-through' de-embedding procedure was used to calibrate out the RF testing fixture effects. The RF testing fixture was designed to a GSG configuration with 150 μm pitch for 40 GHz probes, as shown in the lower right inset of Fig. 2a. The on-chip area S, defined as the in-plane projection area of the tubular structure on the wafer, was calculated without including the testing fixture. Electrical performance could then be extracted based on the impedance (Z) parameter, which was converted from the measured S parameter. By using a high-frequency T-network to model the transformer's performance, the frequency (f) dependent effective self-inductances of the primary (L_p) and secondary (L_s) coils and the mutual inductance (M) are given by $L_p = \mathrm{Im}(Z_{11})/2\pi f$, $L_s = \mathrm{Im}(Z_{22})/2\pi f$ and $M = \mathrm{Im}(Z_{21})/2\pi f$, respectively.

The corresponding turns ratio (n) and the magnetic coupling coefficient (k_{im}) were then calculated by $n=\sqrt{L_p/L_s}$ and $k_m=M/\sqrt{L_pL_s}$. The Q factors of the primary (Q_p) and secondary (Q_s) coils were calculated using $Q_p=\mathrm{Im}(Z_{11})/\mathrm{Re}(Z_{11})$ and $Q_s=\mathrm{Im}(Z_{22})/\mathrm{Re}(Z_{22})$. Note that the turns ratio n is an ideal value, without considering the leakage magnetic flux, which was evaluated in the index of performance $k_{im}n/S$.

Data availability. The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author contributions

X.L. designed and supervised the research. W.H. led the structural designs, mechanical modelling and electromagnetic modelling. W.H. and J.Z. led the fabrication of all samples, with assistance from S.L., M.D.K., M.L. and J.A.M. W.H. and P.F. led the d.c. and RF electrical measurements, with assistance from M.L., D.J.S., J.Z. and S.G. K.W. led the mechanical measurements, with assistance from W.H. and P.F. All authors commented on the paper.

Competing interests

The authors declare no competing interests.

Additional information

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